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FACSIMILE TRANSMISSION

Date: February 11, 2008 **Pages:** 14 (including cover)

To: U.S. Patent Office – Office of Finance – Refund Branch **From:** Brian C. Altmiller

Fax No.: 571-273-6500

Subject: Request for Refund of Overpayment of Fees in Application S/N: 10/790,211

Applicant: AOKI	Atty. Dkt.: 01-562-RCE
Serial No.: 10/790,211	Art Unit: 2815
Filed: March 2, 2004	Examiner: KRAIG, William F.
Title: SEMICONDUCTOR DEVICE HAVING TRENCH GATE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME	

Sirs,

We respectfully request a refund of $50 that was overpaid with our Amendment filed on December 12, 2007. Please note from the attached documentation that the amended total number of claims equals 32, not 33, as reflected in the fee transmittal submitted with the amendment. The amount of $400 was charged to our deposit account no. 50-1147 on December 14, 2007. Therefore, the correct charge for extra claims is $350 (i.e., 7 extra claims over highest paid 25) resulting in an overpayment of $50.

Accordingly, the undersigned hereby requests that $50 be refunded by crediting our Deposit Account No. 50-1147. Acknowledgement of receipt and approval of this request is respectfully requested.

To facilitate a prompt refund, copies of the following are attached hereto for your reference:

(1) Copy of Fee Transmittal filed with the Amendment on December 12, 2007 (1 page);

(2) Copy of Listing of Claims from Amendment filed on December 12, 2007 (pages 1 – 11);

(3) Copy of Deposit Account No. 501147 Statement for December 2007 (page 1).

Respectfully submitted,

Brian C. Altmiller (Reg. No. 37,271)

PAGE 1/14 * RCVD AT 2/11/2008 12:00:24 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-4/10 * DNIS:2736500 * CSID:7037079112 * DURATION (mm-ss):03-20

PTO/SB/17 (12-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Effective on 12/8/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

	Complete If Known
Application Number	10/790,211
Filing Date	March 2, 2004
First Named Inventor	AOKI
Examiner Name	William F. KRAIG
Art Unit	2815
Attorney Docket No.	01-562-RCE

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 400

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 50-1147 Deposit Account Name: Posz Law Group, PLC

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charges fee(s) indicated below, except for the filing fee

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	310	155	510	255	210	105	
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	210	105
Multiple dependent claims	370	185

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
33 - 20 or HP =	8 x	$ 50 =	$ 400

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
4 - 3 or HP =	0 x	$ 0 =	$ 0

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
$	$

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $ ($ for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
- 100 =	/ 50 =	(round up to a whole number) x	=	$0

4. OTHER FEE(S)

Non-English Specification, $130 fee (no small entity discount) — Fees Paid ($)

Other: _____ $

SUBMITTED BY

Signature	Brian Altmiller	Registration No. (Attorney/Agent) 37,271	Telephone (703) 707-9110
Name (Print/Type)	BRIAN C. ALTMILLER		Date 12 December 2007

This collection of information is required by 37 CFR 1.136. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Adjustment date: 02/26/2008 MGEBREH1
12714/2007 PCHOMP 00000012 501147 10790211

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: AOKI	Atty. Dkt.: 01-562-RCE
Serial No.: 10/790,211	Art Unit: 2815
Filed: March 2, 2004	Examiner: William F. KRAIG
Title: SEMICONDUCTOR DEVICE HAVING TRENCH GATE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME	Confirmation No.: 1016

BOX AF
Commissioner for Patents
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Alexandria, VA 22314

Date: 12 December 2007

CERTIFICATE OF FACSIMILE TRANSMISSION			
I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. 571-273-8300 on 12 December 2007, to the Examiner William F. Kraig, GAU 2815.			
Type or printed name	BRIAN C. ALTMILLER		
Signature		Date	12 December 2007

AMENDMENT UNDER 37 CFR 1.116

Sir:

In response to the Office Action mailed **12 September 2007**, the period for response to which extends through **12 December 2007**, please amend the application as follows:

Amendments to the Claims are reflected in the listing of claims that begins on page 1 of this paper.

02/26/2008 MGEBREM1 00000007 501147 10790211
01 FC:1202 350.00 DA

Remarks begin on page 12 of this paper.

LISTING OF CLAIMS:

The present listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a conductive film in the trench on the insulation film; ~~and~~

forming an interlayer over the conductive film; and

annealing the substrate for improvement of reliability of the insulation film at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, ~~and~~

wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius, and

wherein the annealing of the substrate is performed prior to forming the interlayer.

2. (Original) The method according to claim 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

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wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

3. (Cancelled)

4. (Previously Presented) The method according to claim 1, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

5. (Original) The method according to claim 1,

wherein the conductive film is made of doped poly crystalline silicon, and

wherein the insulation film is made of silicon oxide and silicon nitride.

6. (Original) The method according to claim 5, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

7. (Original) The method according to claim 1,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

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wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

8. (Original) The method according to claim 7, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

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9. (Original) The method according to claim 1,

wherein the device includes a cell region and a gate lead wire region,

wherein the cell region includes a plurality of cells, each of which works as a transistor, and

wherein the gate lead wire region includes a gate lead wire.

10. (Original) The method according to claim 9,

wherein the transistor is an N channel type MOSFET, a P channel type MOSFET or an IGBT.

11. (Currently Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a trench having an inner wall in a substrate;

forming an insulation film on the inner wall of the trench;

forming a gate electrode in the trench on the insulation film;

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode;

performing a thermal diffusion process for diffusing the impurity so that a source region adjacent to the trench and disposed on a surface of the substrate is formed; and

annealing the substrate for improvement of reliability of the insulation film at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature,

wherein the substrate is made of silicon, ~~and~~

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wherein the annealing temperature is higher than 1150 degrees Celsius and is equal to or less than 1200 degrees Celsius, and

wherein the annealing is performed prior to performing the thermal diffusion process.

12. (Original) The method according to claim 11,

wherein the thermal diffusion process is performed at a process temperature, and

wherein the annealing temperature in the step of annealing is higher than the process temperature in the step of performing the thermal diffusion process.

13. (Original) The method according to claim 11,

wherein the insulation film includes an oxide-nitride-oxide film and upper and lower oxide films,

wherein the trench includes a sidewall and upper and lower portions,

wherein the oxide-nitride-oxide film is disposed on the sidewall of the trench, the upper oxide film is disposed on the upper portion of the trench, and the lower oxide film is disposed on the lower portion of the trench,

wherein the oxide-nitride-oxide film includes a silicon oxide film, a silicon nitride film and another silicon oxide film, and

wherein the upper and lower oxide films are made of silicon oxide.

14. (Original) The method according to claim 13, further comprising the step of:

forming a source region having a contact surface between the source region and the substrate, which is disposed near the trench and is almost parallel to the substrate,

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wherein the conductive film in the trench provides a gate electrode,

wherein the gate electrode includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section,

wherein the canopy of the gate electrode has an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and

wherein the predetermined distance is predetermined not to prevent the source region from forming.

15. (Previously Presented) The method according to claim 14,

wherein the distance between the edge of the canopy and the edge of the opening of the trench is in a range between 0.05 micrometers and 0.1 micrometers.

16. (Previously Presented) The method according to claim 11,

wherein the substrate is annealed in an inert gas atmosphere in the step of annealing.

17-25. (Canceled)

26. (Previously Presented) The method according to claim 1, further comprising forming an oxide film on the conductive film before the annealing of the substrate.

27. (Previously Presented) The method according to claim 26, wherein the oxide film covers the conductive film and the substrate.

28. (Previously Presented) The method according to claim 27, wherein the annealing of the substrate is performed for a predetermined time in a range between 10 minutes and 30 minutes.

29. (Previously Presented) The method according to claim 11, further comprising forming an oxide film on the conductive film before the annealing of the substrate.

30. (Previously Presented) The method according to claim 29, wherein the oxide film covers the conductive film and the substrate.

31. (Previously Presented) The method according to claim 30, wherein the annealing of the substrate is performed for a predetermined time in a range between 10 minutes and 30 minutes.

32. (New) The method according to claim 1, wherein the interlayer comprises borophosphosilicate glass

34. (New) The method according to claim 2, wherein the annealing is performed prior to forming the source region.

35. (New) The method according to claim 2, wherein the source region is an N^+ source region.

36. (New) The method according to claim 2, further comprising forming a body region in the substrate and adjacent to the source region.

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37. (New) The method according to claim 36,

wherein the source region is an N^+ type source region, and

wherein the body region is a P type body region.

38. (New) The method according to claim 11, wherein the source region is an N^+ source region.

39. (New) The method according to claim 11, wherein the performing of the thermal diffusion process for diffusing the impurity also operates so that a body region is formed adjacent to the source region in the substrate.

40. (New) The method according to claim 39, wherein the annealing is performed prior to performing the thermal diffusion process.

41. (New) The method according to claim 40,

wherein the source region is an N^+ type source region, and

wherein the body region is a P type body region.

42. (New) The method according to claim 11, further comprising

forming an interlayer over the gate electrode,

wherein the annealing of the substrate is performed prior to forming the interlayer

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43. (New) The method according to claim 42, wherein the interlayer comprises borophosphosilicate glass.

Deposit Account Statement

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Deposit Account Statement

Requested Statement Month:	December 2007
Deposit Account Number:	501147
Name:	POSZ LAW GROUP, PLC
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DATE	SEQ	POSTING REF TXT	ATTORNEY DOCKET NBR	FEE CODE	AMT	BAL
12/04	9645	E-REPLENISHMENT		9203	-$1,000.00	$5,071.83
12/10	1	11108758	01-801	1251	$120.00	$4,951.83
12/11	1	11244177	01-1019	1251	$120.00	$4,831.83
12/11	27	11004937	12-057	1464	$130.00	$4,701.83
12/11	28	11004937	12-057	1801	$810.00	$3,891.83
12/11	12830	E-REPLENISHMENT		9203	-$1,000.00	$4,891.83
12/12	2416	E-REPLENISHMENT		9203	-$5,000.00	$9,891.83
12/13	44	11596647	24-042-TN	8021	$40.00	$9,851.83
12/14	13	10790211	01-562	1202	$400.00	$9,451.83
12/14	5	11795009		9204	-$250.00	$9,701.83
12/14	39	11455852	02-165	1253	$1,050.00	$8,651.83
12/14	52	11199132	01-1003	2402	$255.00	$8,396.83
12/14	406	11922088	49-016-TN	2615	$225.00	$8,171.83
12/17	7	10891478	113708.131	2401	$255.00	$7,916.83
12/17	8	10891478	113708.131	2251	$60.00	$7,856.83
12/17	10959	10577135	VX062735 PCT	8021	$40.00	$7,816.83
12/18	18	10651248	26H-005	1801	$810.00	$7,006.83
12/18	19	10651248	26H-005	1251	$120.00	$6,886.83
12/18	3	11653413	26C-010-TN-CON	1814	$130.00	$6,756.83
12/21	4508	76606302	112033.343	7004	$300.00	$6,456.83
12/21	35	11004979	01-757	1251	$120.00	$6,336.83
12/21	64	11073621	11-303	1201	$420.00	$5,916.83
12/26	15896	77359216	112176.133	7001	$325.00	$5,591.83
12/26	16455	2784269	9112033.024	8521	$40.00	$5,551.83

PTO/SB/06 (12-04)
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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number: 10/790,121

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))							
SEARCH FEE (37 CFR 1.16(k), (l), or (m))							
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))							
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *				OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *				OR		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
			TOTAL			TOTAL	

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

12/12/07

AMENDMENT A	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 33	Minus	** 25	= 8	x25 =		OR	x50 =	400.00
Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	=	x100 =		OR	x200 =	
Application Size Fee (37 CFR 1.16(s))							OR		
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	400.00

AMENDMENT B	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 32	Minus	** 25	= 7	x =		OR	x 50 =	350
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))							OR		
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	350

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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